ADC and DAC

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1 Digital to Analog Converter

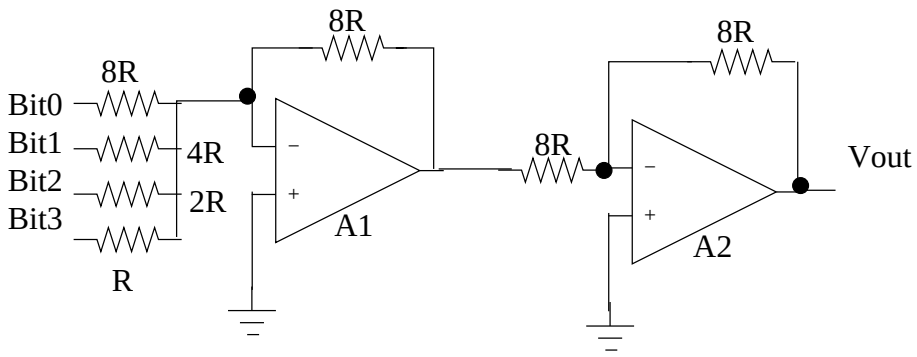

Figure 1: Digital to Analog converter

Refer to the figure 1 on page 1. This is one way of implementing a digital to analog converter. It uses operational amplifers. Details of the ckt configuration are given below.

1. Circuit in figure 1 shows a 4 bit DAC using *weighted code technique.*
2. Amplifier A1 is in inverting adder mode.
3. Input to A1 are four resistors of values as shown.
4. At bit-0 input (least significant bit) gain is -1.
5. At bit-1 input, gain is -2.
6. At bit-2 input, gain is -4.
7. At bit-3 input,(most significant bit) gain is -8.

8. Notice the gain is decided by resistors and is relevant to the bit significance.

9. Gains work like the weights for the corrosponding bits and finally voltages are added.

10. Output voltage is negative but is analog equivalent of the input binary number.

11. To get +ve output voltage as desired, we use A2 which is unity gain inverting amplifier.

12. Thus output of A2 is equivalent analog voltage of input binary number.

2 Analog to Digital Converter

2.1 Working of ADC:

Refer to the figure 2. To find the digital (binary) equivalent of the input analog voltage, following steps are executed by the ADC chip. This is known as **Successive Approximation Register** technique.

1. Logic block loads a binary number (normally half the range) to SA register.

2. Analog equivalent voltage of the above number is given at the DAC output.

3. Incoming analog voltage and the DAC output (above) are compared by a comparator.

4. Output of the comparator is either **High** or **Low**.

   (a) If **High**, DAC output is less than the incoming voltage.

   (b) If **Low**, DAC output is more than the incoming voltage.

5. Depending upon the comparator output, logic block increments or decrements the binary number loaded in the SAR. Here, the logic is as below:

   Comparator output, if high , logic will go to the upper half of the range.

   Load the midvalue of the upper half to the SAR.

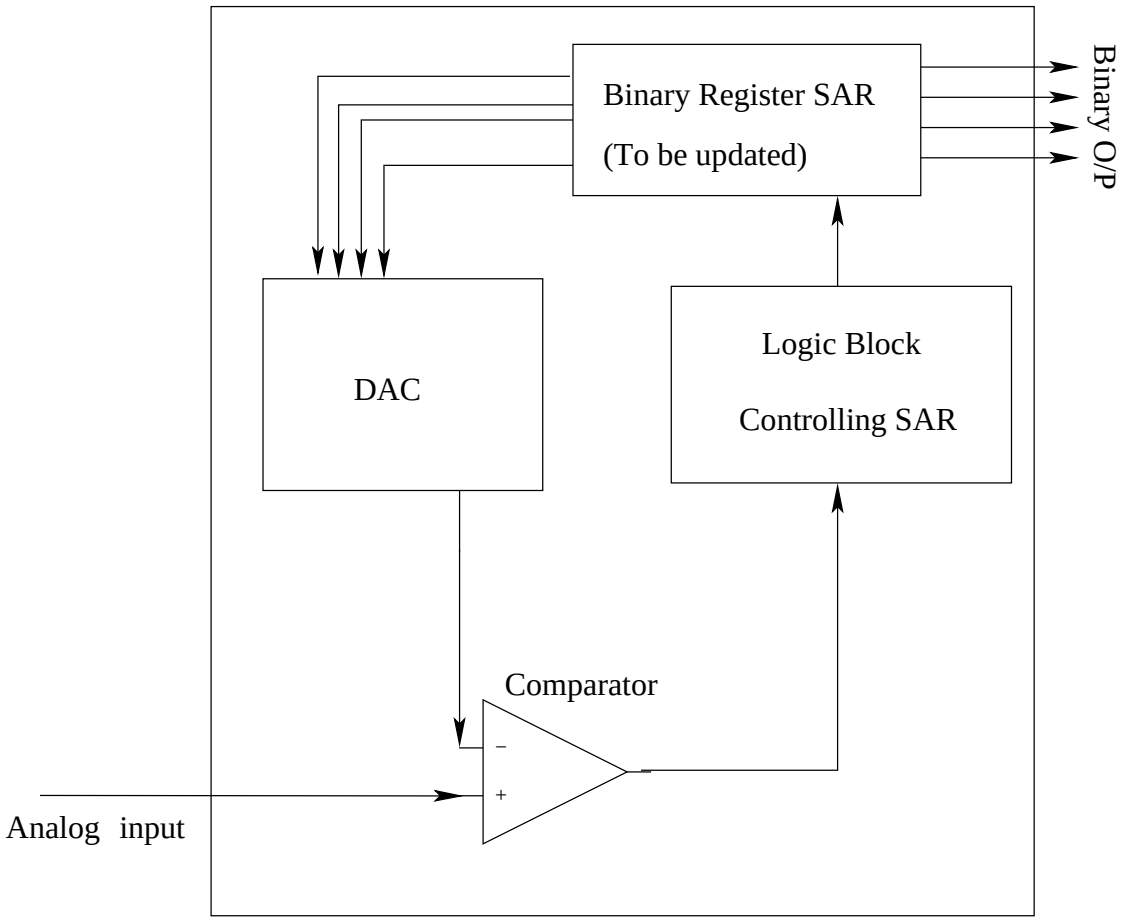

Figure 2: ADC block diagram

Comparator output, if low , logic will go to the lower half of the range.

Load the value of the lower half to the SAR.

New binary value in SAR will generate new analog voltage at DAC output.

6. DAC output is again compared with the incoming signal voltage.

7. This process is iterated n times where n is number of bits in the output binary number.

8. After n such iterations, the number in the SAR is latched and declared as the equivalent binary output.